CLAIMS

We claim:

1. An apparatus comprising:

a package, said package comprising a plurality of shelves;

a first semiconductor die electrically coupled to at least one of said shelves; and,

a second semiconductor die electrically coupled to at least one of said shelves, wherein said second semiconductor die is above said first semiconductor die.

2. The apparatus of claim 1 wherein said package comprises a ceramic pin grid array (PGA) package.

3. The apparatus of claim 1 wherein said package comprises a plastic pin grid array (PPGA) package.

4. The apparatus of claim 1 wherein said first semiconductor die is a central processing unit (CPU) die.

5. The apparatus of claim 4 wherein said second semiconductor die is a memory cache.

6. The apparatus of claim 1 wherein said package has a single chip footprint.

7. The apparatus of claim 1 wherein said first semiconductor die is wire bonded to said at least one shelf.

8. The apparatus of claim 7 wherein said second semiconductor die is wire bonded to said at least one shelf.

9. The apparatus of claim 1 wherein said second semiconductor die is electrically attached to a substrate and said substrate is wire bonded to said at least one shelf.

10. The apparatus of claim 9 wherein said second semiconductor die is wire bonded to said substrate.

11. The apparatus of claim 9 wherein said second semiconductor die is electrically attached to said substrate by solder bumps.

12. The apparatus of claim 1 further comprising an encapsulant filling said package above said second semiconductor die.

13. The apparatus of claim 12 wherein said second semiconductor die is attached to said at least one shelf such that an open cavity protects said first semiconductor die.

14. An apparatus comprising:

a plurality of shelves, said package for housing a plurality of semiconductor dies in a vertically stacked position such that said package has a single chip package footprint;

a first semiconductor die electrically coupled to at least one of said shelves; and,

a second semiconductor die electrically coupled to at least on of said shelves, wherein said second semiconductor doe as above said first semiconductor die.

15. The apparatus of claim 14 wherein said package comprises a ceramic pin grid array (PGA) package.

16. The apparatus of claim 14 wherein said package comprises a plastic pin grid array (PPGA) package.

17. The apparatus of claim 14 wherein said first semiconductor die is a central processing unit (CPU) die.

18. The apparatus of claim 17 wherein said second semiconductor die is a memory cache.

19. The apparatus of claim 14 further comprising an encapsulant filling said package above said second semiconductor die.

20. The apparatus of claim 19 wherein said second semiconductor die is attached to said at least one shelf such that an open cavity protects said first semiconductor die.

21. A method constructing a multi-chip package, comprising:

placing a fist chip package on a first shelf;

electrically attaching said first chip package to said first shelf;

placing a second chip package on a second shelf wherein said second shelf is stacked above said first shelf; and,

electrically attaching said second chip package to said second shelf.

22. The method of claim 21 further comprising the step of filling said package above said second chip package with an encapsulant.

23. The method of claim 22 wherein said step of placing a second chip package on a second shelf further comprises placing a second chip package on a second shelf with a sealer such that a sealed open cavity below said second shelf protects said first chip package.

24. The method of claim 21 wherein said step of placing a first chip package further comprises placing CPU chip package on a first shelf.

25. The method of claim 21 wherein said step of placing a second chip package further comprises placing a memory cache on a second shelf.

26. The method of claim 21 wherein said step of electrically attaching said first chip package further comprises wire bonding said first chip package to said first shelf.

27. The method of claim 21 wherein said step of electrically attaching said second chip package further comprises wire bonding said second chip package to said second shelf.